AMENDMENTS TO THE CLAIMS

1. (Currently Amended) An apparatus comprising:

a display controller;

an internal frame buffer coupled to the display controller; and

a control circuitry to copy display data from an external frame buffer to the internal frame buffer, wherein the display data copied into the internal frame buffer is the same display data read by the display controller from the external frame buffer, wherein after the display data is copied, the same display data is located in the internal frame buffer and the external frame buffer until a new frame is available in the external frame buffer.

2. (Original) The apparatus of claim 1, wherein the display data is copied into the internal frame buffer simultaneously with the display controller reading the display data from the external frame buffer.

3. (Original) The apparatus of claim 1, wherein the display controller reads the display data from the internal frame buffer until the display controller receives a signal indicating that the external frame buffer contains the most recent display data.

4. (Original) The apparatus of claim 1, wherein the display controller reads the display data from the internal frame buffer at least one time after a new frame display refresh operation.

5. (Original) The apparatus of claim 1, wherein the display controller, the internal frame buffer and the control circuitry are disposed on a single graphics chip and the external frame buffer is disposed on another chip separate from the graphics chip.

6. (Original) The apparatus of claim 1, wherein the display controller, the internal frame buffer and the control circuitry are disposed on a single processor chip.

7. (Original) The apparatus of claim 1, wherein the control circuitry comprises at least one register to hold at least one data transaction of display data.

8. (Original) The apparatus of claim 1, wherein the control circuitry is to generate a write signal to be used by the internal frame buffer based on an external memory read signal and a memory clock signal.

9. (Currently Amended) A system comprising:

a processor;

a display device;

a graphics chip coupled between the processor and the display device, the graphics chip including a display controller, an internal memory array and data copy circuitry; and

an external memory array disposed on another chip separate from the graphics chip, wherein the data copy circuitry is coupled between the external memory array and the internal memory array to enable data from the external memory array to be copied to the internal memory array during a new frame display refresh operation,

wherein after the display data is copied, the same display data is located in the internal frame buffer and the external frame buffer until a new frame is available in the external frame buffer, and

wherein subsequent display refresh operations are accomplished by the display controller retrieving data from the internal memory array until ~~a~~ the new frame is available in the external memory array.

10. (Original) The system of claim 9, wherein the display controller retrieves the data from the external memory array simultaneously with copy of the data from the external memory array to the internal memory array.

11. (Original) The system of claim 9, wherein the display data copied into the internal memory array is the same display data read by the display controller from the external memory array.

12. (Original) The system of claim 9, further comprising a graphics generator disposed on the graphics chip.

13. (Original) The system of claim 9, wherein the data copy circuitry comprises at least one register to hold at least one data transaction of display data.

14. (Original) The system of claim 9, wherein the data copy circuitry generates a write signal to be used by the internal memory array based on an external memory read signal and a memory clock signal.

15. (Original) The system of claim 9, further comprising:

a portable power source coupled to power the display controller, the internal memory array, the external memory array and the data copy circuitry.

16. (Currently Amended) A method comprising:

reading display data from an external frame buffer by a display controller during a new frame display refresh operation; and

loading a copy of the display data from the external frame buffer to an internal frame buffer during the new frame display refresh operation, such that the same display data is located in the internal frame buffer and the external frame buffer until a new frame is available in the external frame buffer.

17. (Original) The method of claim 16, further comprising:

determining if a new frame is available in the external frame buffer; and

reading the display data in the internal frame buffer by the display controller during subsequent display refresh operations if a new frame is not available in the external frame buffer.

18. (Original) The method of claim 17, wherein the display data from the external frame buffer includes rendered graphics objects or an entire frame.

19. (Original) The method of claim 16, wherein reading of the data from the external frame buffer by the display controller is executed simultaneously with loading of the data from the external frame buffer to the internal frame buffer.

20. (Original) The method of claim 16, wherein loading of the data from the external frame buffer to the internal frame buffer is accomplished using data copy circuitry.

21. (Original) The method of claim 20, further comprising:

disposing the display controller, the internal frame buffer and the data copy circuitry on a single graphics chip; and

disposing the external frame buffer on another chip separate from the graphics chip.

22. (Original) The method of claim 16, wherein loading of the data from the external frame buffer to the internal frame buffer further comprises:

temporarily storing at least one data transaction of the display data in a register; and

writing the stored data into the internal frame buffer based on an external memory read signal.